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CMOS Special Purpose Subsystem Formulas

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List of 20 CMOS Special Purpose Subsystem Formulas

CMOS Special Purpose Subsystem

1) Capacitance of External Load

$$fx \quad C_{out} = h \cdot C_{in}$$

Open Calculator 

$$ex \quad 42pF = 0.84 \cdot 50pF$$

2) Change in Frequency of Clock

$$fx \quad \Delta f = \frac{h}{f_{abs}}$$

Open Calculator 

$$ex \quad 0.084Hz = \frac{0.84}{10Hz}$$

3) Change in Phase of Clock

$$fx \quad \Delta \Phi_f = \frac{\Phi_{out}}{f_{abs}}$$

Open Calculator 

$$ex \quad 2.989 = \frac{29.89}{10Hz}$$



4) Delay for Two Inverters in Series

$$f_x D_C = h_1 + h_2 + 2 \cdot P_{inv}$$

[Open Calculator !\[\]\(cbe80b694ebd74fcfe136a095b608235_img.jpg\)](#)

$$ex \ 0.05s = 2.14mW + 31mW + 2 \cdot 8.43mW$$

5) Fanout of Gate

$$f_x \ h = \frac{f}{g}$$

[Open Calculator !\[\]\(3e2231b1ad3ca8da8658228c00dd08e0_img.jpg\)](#)

$$ex \ 0.838235 = \frac{3.99}{4.76}$$

6) Feedback Clock PLL

$$f_x \ \Delta\Phi_c = \Delta\Phi_{in} - \Delta\Phi_{er}$$

[Open Calculator !\[\]\(0d5ec72f61334709c3fc9450209b754f_img.jpg\)](#)

$$ex \ 1.21 = 5.99 - 4.78$$

7) Gate Delay

$$f_x \ G_d = 2^{N_{sr}}$$

[Open Calculator !\[\]\(b64b40baaee5acddc1eab8538ba84754_img.jpg\)](#)

$$ex \ 4.594793s = 2^{2.2}$$

8) Input Clock Phase PLL

$$f_x \ \Delta\Phi_{in} = \frac{\Phi_{out}}{H_s}$$

[Open Calculator !\[\]\(aff7c69c44a5e015f18c35867ef3f5c3_img.jpg\)](#)

$$ex \ 5.98998 = \frac{29.89}{4.99}$$



9) Inverter Electric Effort 1 

$$fx \quad h_1 = D_C - (h_2 + 2 \cdot P_{inv})$$

[Open Calculator !\[\]\(e78f798d4ea5c530c9db49e7d26e6b95_img.jpg\)](#)

$$ex \quad 2.14mW = 0.05s - (31mW + 2 \cdot 8.43mW)$$

10) Inverter Electric Effort 2 

$$fx \quad h_2 = D_C - (h_1 + 2 \cdot P_{inv})$$

[Open Calculator !\[\]\(05be7c7a8995decd503647c99211f7c2_img.jpg\)](#)

$$ex \quad 31mW = 0.05s - (2.14mW + 2 \cdot 8.43mW)$$

11) Inverter Power 

$$fx \quad P_{inv} = \frac{D_C - (h_1 + h_2)}{2}$$

[Open Calculator !\[\]\(fe3aebe81acea8d45108cd2768939da7_img.jpg\)](#)

$$ex \quad 8.43mW = \frac{0.05s - (2.14mW + 31mW)}{2}$$

12) Output Clock Phase PLL 

$$fx \quad \Phi_{out} = H_s \cdot \Delta\Phi_{in}$$

[Open Calculator !\[\]\(899d8b7697d64725bf017d3296cfcf1b_img.jpg\)](#)

$$ex \quad 29.8901 = 4.99 \cdot 5.99$$

13) PLL Phase Detector Error 

$$fx \quad \Delta\Phi_{er} = \Delta\Phi_{in} - \Delta\Phi_c$$

[Open Calculator !\[\]\(40770d9ed6ed4f1222ebf89a1396e8b2_img.jpg\)](#)

$$ex \quad 4.78 = 5.99 - 1.21$$



14) Power Consumption of Chip

$$fx \quad P_{\text{chip}} = \frac{\Delta T}{\Theta_j}$$

[Open Calculator !\[\]\(e2376d476d06eb31946dc01a69a4403a_img.jpg\)](#)

$$ex \quad 0.797342\text{mW} = \frac{2.4\text{K}}{3.01\text{K/mW}}$$

15) Series Resistance from Die to Package

$$fx \quad \Theta_{jp} = \Theta_j - \Theta_{pa}$$

[Open Calculator !\[\]\(0b5e7e25e8775f7e7e80906ada4f0021_img.jpg\)](#)

$$ex \quad 1.6\text{K/mW} = 3.01\text{K/mW} - 1.41\text{K/mW}$$

16) Series Resistance from Package to Air

$$fx \quad \Theta_{pa} = \Theta_j - \Theta_{jp}$$

[Open Calculator !\[\]\(bd3b31712ad9bab5a241210fa6925cdd_img.jpg\)](#)

$$ex \quad 1.41\text{K/mW} = 3.01\text{K/mW} - 1.60\text{K/mW}$$

17) Stage Effort

$$fx \quad f = h \cdot g$$

[Open Calculator !\[\]\(7bc43b319a082987e20f7bf78f4bab80_img.jpg\)](#)

$$ex \quad 3.9984 = 0.84 \cdot 4.76$$

18) Temperature Difference between Transistors

$$fx \quad \Delta T = \Theta_j \cdot P_{\text{chip}}$$

[Open Calculator !\[\]\(4a7b4ce770af8456e11a71f9565c8c2b_img.jpg\)](#)

$$ex \quad 2.39897\text{K} = 3.01\text{K/mW} \cdot 0.797\text{mW}$$



19) Thermal Resistance between Junction and Ambient

$$\text{fx } \Theta_j = \frac{\Delta T}{P_{\text{chip}}}$$

[Open Calculator !\[\]\(d3fb9f94af8b26d1c844efa9a98805b0_img.jpg\)](#)

$$\text{ex } 3.011292\text{K/mW} = \frac{2.4\text{K}}{0.797\text{mW}}$$

20) Transfer Function of PLL

$$\text{fx } H_s = \frac{\Phi_{\text{out}}}{\Delta\Phi_{\text{in}}}$$

[Open Calculator !\[\]\(e1d6102fe77919492c04879c8450f1f5_img.jpg\)](#)

$$\text{ex } 4.989983 = \frac{29.89}{5.99}$$



Variables Used







- C_{in} Input Capacitance (Picofarad)
- C_{out} Capacitance of External Load (Picofarad)
- D_C Delay of Chains (Second)
- f Stage Effort
- f_{abs} Absolute Frequency (Hertz)
- g Logical Effort
- G_d Gate Delay (Second)
- h Fanout
- h_1 Electric Effort 1 (Milliwatt)
- h_2 Electric Effort 2 (Milliwatt)
- H_s Transfer Function PLL
- N_{sr} N Bit SRAM
- P_{chip} Power Consumption of Chip (Milliwatt)
- P_{inv} Inverter Power (Milliwatt)
- Δf Change in Frequency of Clock (Hertz)
- ΔT Temperature Difference Transistors (Kelvin)
- $\Delta\Phi_c$ Feedback Clock PLL
- $\Delta\Phi_{er}$ PLL Error Detector
- $\Delta\Phi_f$ Change in Phase of Clock
- $\Delta\Phi_{in}$ Input Reference Clock Phase
- Θ_j Thermal Resistance between junction and Ambient (Kelvin per Milliwatt)



- Θ_{jp} Series Resistance from Die to Package (*Kelvin per Milliwatt*)
- Θ_{pa} Series Resistance from Package to Air (*Kelvin per Milliwatt*)
- Φ_{out} PLL Output Clock Phase








Constants, Functions, Measurements used

- **Measurement: Time** in Second (s)
Time Unit Conversion 
- **Measurement: Temperature** in Kelvin (K)
Temperature Unit Conversion 
- **Measurement: Power** in Milliwatt (mW)
Power Unit Conversion 
- **Measurement: Frequency** in Hertz (Hz)
Frequency Unit Conversion 
- **Measurement: Capacitance** in Picofarad (pF)
Capacitance Unit Conversion 
- **Measurement: Thermal Resistance** in Kelvin per Milliwatt (K/mW)
Thermal Resistance Unit Conversion 



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