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Array Datapath Subsystem Formulas

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List of 19 Array Datapath Subsystem Formulas

Array Datapath Subsystem

1) Area of Memory Cell

$$\text{fx } A_{\text{bit}} = \frac{E \cdot A}{f_{\text{abs}}}$$

[Open Calculator !\[\]\(a870788d6ed9b8fd294b7654a8c8526b_img.jpg\)](#)

$$\text{ex } 47.71976\text{mm}^2 = \frac{0.88 \cdot 542.27\text{mm}^2}{10\text{Hz}}$$

2) Area of Memory Containing N Bits

$$\text{fx } A = \frac{A_{\text{bit}} \cdot f_{\text{abs}}}{E}$$

[Open Calculator !\[\]\(c50c8b7b2cc2cf9ff925edec0ee94c0d_img.jpg\)](#)

$$\text{ex } 542.2727\text{mm}^2 = \frac{47.72\text{mm}^2 \cdot 10\text{Hz}}{0.88}$$

3) Array Efficiency

$$\text{fx } E = \frac{A_{\text{bit}} \cdot f_{\text{abs}}}{A}$$

[Open Calculator !\[\]\(f60b7a900783ac3fd531bfd9c111be6d_img.jpg\)](#)

$$\text{ex } 0.880004 = \frac{47.72\text{mm}^2 \cdot 10\text{Hz}}{542.27\text{mm}^2}$$



4) Bit Capacitance

$$f_x \quad C_{\text{bit}} = \left(\frac{V_{\text{dd}} \cdot C_{\text{cell}}}{2 \cdot \Delta V} \right) - C_{\text{cell}}$$

[Open Calculator !\[\]\(cbe80b694ebd74fcfe136a095b608235_img.jpg\)](#)

$$ex \quad 12.38714\text{pF} = \left(\frac{2.58\text{V} \cdot 5.98\text{pF}}{2 \cdot 0.42\text{V}} \right) - 5.98\text{pF}$$

5) Carry-Incrementor Adder Delay

$$f_x \quad T_{\text{inc}} = t_{\text{pg}} + t_{\text{gp}} + (K - 1) \cdot T_{\text{ao}} + T_{\text{xor}}$$

[Open Calculator !\[\]\(3e2231b1ad3ca8da8658228c00dd08e0_img.jpg\)](#)

$$ex \quad 27.3\text{ns} = 8.01\text{ns} + 5.5\text{ns} + (7 - 1) \cdot 2.05\text{ns} + 1.49\text{ns}$$

6) Carry-Looker Adder Delay

 f_x
[Open Calculator !\[\]\(0d5ec72f61334709c3fc9450209b754f_img.jpg\)](#)

$$t_{\text{cla}} = t_{\text{pg}} + t_{\text{gp}} + ((n - 1) + (K - 1)) \cdot T_{\text{ao}} + T_{\text{xor}}$$

$$ex \quad 29.35\text{ns} = 8.01\text{ns} + 5.5\text{ns} + ((2 - 1) + (7 - 1)) \cdot 2.05\text{ns} + 1.49\text{ns}$$

7) Carry-Ripple Adder Critical Path Delay

$$f_x \quad T_{\text{ripple}} = t_{\text{pg}} + (N_{\text{gates}} - 1) \cdot T_{\text{ao}} + T_{\text{xor}}$$

[Open Calculator !\[\]\(84f47badaad7772cd95667a7c387a639_img.jpg\)](#)

$$ex \quad 30\text{ns} = 8.01\text{ns} + (11 - 1) \cdot 2.05\text{ns} + 1.49\text{ns}$$



8) Carry-Skip Adder Delay

fx

Open Calculator 

$$T_{\text{skip}} = t_{\text{pg}} + 2 \cdot (n - 1) \cdot T_{\text{ao}} + (K - 1) \cdot t_{\text{mux}} + T_{\text{xor}}$$

$$\text{ex } 34.3\text{ns} = 8.01\text{ns} + 2 \cdot (2 - 1) \cdot 2.05\text{ns} + (7 - 1) \cdot 3.45\text{ns} + 1.49\text{ns}$$

9) Cell Capacitance

fx

Open Calculator 

$$C_{\text{cell}} = \frac{C_{\text{bit}} \cdot 2 \cdot \Delta V}{V_{\text{dd}} - (\Delta V \cdot 2)}$$

$$\text{ex } 5.976552\text{pF} = \frac{12.38\text{pF} \cdot 2 \cdot 0.42\text{V}}{2.58\text{V} - (0.42\text{V} \cdot 2)}$$

10) Critical Delay in Gates

fx

Open Calculator 

$$T_{\text{gd}} = t_{\text{pg}} + (n + (K - 2)) \cdot T_{\text{ao}} + t_{\text{mux}}$$

$$\text{ex } 25.81\text{ns} = 8.01\text{ns} + (2 + (7 - 2)) \cdot 2.05\text{ns} + 3.45\text{ns}$$

11) Ground Capacitance

fx

Open Calculator 

$$C_{\text{gnd}} = \left(\frac{V_{\text{agr}} \cdot C_{\text{adj}}}{V_{\text{tm}}} \right) - C_{\text{adj}}$$

$$\text{ex } 2.980392\text{pF} = \left(\frac{17.5\text{V} \cdot 8\text{pF}}{12.75\text{V}} \right) - 8\text{pF}$$



12) Group Propagation Delay

$$fx \quad t_{pg} = t_{tree} - (\log 2(f_{abs}) \cdot T_{ao} + T_{xor})$$

[Open Calculator !\[\]\(e2376d476d06eb31946dc01a69a4403a_img.jpg\)](#)

$$ex \quad 8.000047ns = 16.3ns - (\log 2(10Hz) \cdot 2.05ns + 1.49ns)$$

13) K-Input 'And' Gate

$$fx \quad K = \frac{N_{carry}}{n}$$

[Open Calculator !\[\]\(0b5e7e25e8775f7e7e80906ada4f0021_img.jpg\)](#)

$$ex \quad 7 = \frac{14}{2}$$

14) Multiplexer Delay

 fx
[Open Calculator !\[\]\(bd3b31712ad9bab5a241210fa6925cdd_img.jpg\)](#)

$$t_{mux} = \frac{T_{skip} - (t_{pg} + (2 \cdot (n - 1) \cdot T_{ao}) - T_{xor})}{K - 1}$$

$$ex \quad 3.946667ns = \frac{34.3ns - (8.01ns + (2 \cdot (2 - 1) \cdot 2.05ns) - 1.49ns)}{7 - 1}$$

15) N-Bit Carry-Skip Adder

$$fx \quad N_{carry} = n \cdot K$$

[Open Calculator !\[\]\(e50091943b385fe16d3277389202856f_img.jpg\)](#)

$$ex \quad 14 = 2 \cdot 7$$




16) N-Input 'And' Gate 

$$\text{fx } n = \frac{N_{\text{carry}}}{K}$$

Open Calculator 


$$\text{ex } 2 = \frac{14}{7}$$

17) Tree Adder Delay 

$$\text{fx } t_{\text{tree}} = t_{\text{pg}} + \log 2(f_{\text{abs}}) \cdot T_{\text{ao}} + T_{\text{xor}}$$

Open Calculator 

$$\text{ex } 16.30995\text{ns} = 8.01\text{ns} + \log 2(10\text{Hz}) \cdot 2.05\text{ns} + 1.49\text{ns}$$

18) Voltage Swing On Bitline 

$$\text{fx } \Delta V = \left(\frac{V_{\text{dd}}}{2} \right) \cdot \frac{C_{\text{cell}}}{C_{\text{cell}} + C_{\text{bit}}}$$

Open Calculator 

$$\text{ex } 0.420163\text{V} = \left(\frac{2.58\text{V}}{2} \right) \cdot \frac{5.98\text{pF}}{5.98\text{pF} + 12.38\text{pF}}$$

19) 'XOR' Delay 

$$\text{fx } T_{\text{xor}} = T_{\text{ripple}} - (t_{\text{pg}} + (N_{\text{gates}} - 1) \cdot T_{\text{ao}})$$

Open Calculator 

$$\text{ex } 1.49\text{ns} = 30\text{ns} - (8.01\text{ns} + (11 - 1) \cdot 2.05\text{ns})$$



Variables Used






- **A** Area of Memory Cell (*Square Millimeter*)
- **A_{bit}** Area of One Bit Memory Cell (*Square Millimeter*)
- **C_{adj}** Adjacent Capacitance (*Picofarad*)
- **C_{bit}** Bit Capacitance (*Picofarad*)
- **C_{cell}** Cell Capacitance (*Picofarad*)
- **C_{gnd}** Ground Capacitance (*Picofarad*)
- **E** Array Efficiency
- **f_{abs}** Absolute Frequency (*Hertz*)
- **K** K-Input AND Gate
- **n** N-Input AND Gate
- **N_{carry}** N-bit Carry Skip Adder
- **N_{gates}** Gates on Critical Path
- **T_{ao}** AND-OR Gate Delay (*Nanosecond*)
- **t_{cla}** Carry-Looker Adder Delay (*Nanosecond*)
- **T_{gd}** Critical Delay in Gates (*Nanosecond*)
- **t_{gp}** Group Propagation Delay (*Nanosecond*)
- **T_{inc}** Carry-Incrementor Adder Delay (*Nanosecond*)
- **t_{mux}** Multiplexer Delay (*Nanosecond*)
- **t_{pg}** Propagation Delay (*Nanosecond*)
- **T_{ripple}** Ripple Time (*Nanosecond*)
- **T_{skip}** Carry-Skip Adder Delay (*Nanosecond*)



- t_{tree} Tree Adder Delay (Nanosecond)
- T_{xor} XOR Delay (Nanosecond)
- V_{agr} Agressor Voltage (Volt)
- V_{dd} Positive Voltage (Volt)
- V_{tm} Victim Voltage (Volt)
- ΔV Voltage Swing on Bitline (Volt)



Constants, Functions, Measurements used

- **Function:** **log2**, $\log_2(\text{Number})$
Binary logarithm function (base 2)
- **Measurement:** **Time** in Nanosecond (ns)
Time Unit Conversion 
- **Measurement:** **Area** in Square Millimeter (mm^2)
Area Unit Conversion 
- **Measurement:** **Frequency** in Hertz (Hz)
Frequency Unit Conversion 
- **Measurement:** **Capacitance** in Picofarad (pF)
Capacitance Unit Conversion 
- **Measurement:** **Electric Potential** in Volt (V)
Electric Potential Unit Conversion 



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- [CMOS Delay Characteristics Formulas](#) 
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